UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/873,110	06/01/2001	Eiji Oki	Poly-21/APP	1657

26479 7590 10/28/2004

STRAUB & POKOTYLO
620 TINTON AVENUE
BLDG. B, 2ND FLOOR
TINTON FALLS, NJ 07724

EXAMINER	
MOORE, IAN N	

ART UNIT	PAPER NUMBER
2661	

DATE MAILED: 10/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/873,110	OKI ET AL.	
	Examiner	Art Unit	
	Ian N Moore	2661	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *the application filed on 1-16-2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *8/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for domestic priority under 35 U.S.C. 119(e) is acknowledged. However, it is suggested to incorporate the serial number of the provisional application in the priority claim section, page 1, of the specification.

Claim Objections

2. Claim 5 is objected to because of the following informalities: claim 5 recites an acronym "DRRM" and "iSLIP" in line 3. For clarity, it is suggested to describe the acronyms when reciting for the first time. Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claim 29 is rejected under 35 U.S.C. 102(e) as being anticipated by Golla (U.S. 2002/0176431A1).

Regarding claim 29, Golla discloses a machine-readable medium for use with a switch (see FIG. 1, network switch element 10) including a first number of output ports (see FIG. 1, Egress ports 15-1 to 15-N), a second number of input ports (see FIG. 1, ingress ports

18-1 to 18-N), and the first number of virtual output queues (see FIG. 1, VOQ-1 to VOQ-N) associated with each of the second number of input ports (see FIG. 1, each VOQ is coupled to each ingress port), and a third number of subschedulers (see FIG. 1, a combined system of ingress servers/arbiters 19-1 to 19-H and egress servers/arbiters 14-1 to 14-H; see FIG. 5), the a machine-readable medium having stored thereon:

a first indicator (see FIG. 8, step 142, request matrix R; see FIG. 12 B, request matrix), associated with each of the virtual output queues (see FIG. 12b, the request matrix contains/associates with each VOQ), for indicating whether the virtual output queue is storing a cell awaiting dispatch arbitration (see FIG. 12C, the requests in the request matrix indicates the transmission units waiting to be served/granted by the server/scheduler, and each VOQ stores the transmission units; see page 6, paragraph 65-66; see page 7, paragraph 85-86; page 8, paragraph 87-89); and

a second indicator (see FIG. 12B, the a combined matrix of Grants Matrix and scheduling matrix, see FIG. 8, step 146), for each of the subschedulers (see FIG. 12B, the combined matrix contains/associates with each ingress/egress server), indicating whether the subscheduler is reserved or available (see FIG. 12C, the combined matrix is used at the server/arbiter to indicate/determine whether to accept/grant the request, and the request is used to determine whether there is match with predetermine/stored/reserved output port in the server or no match (i.e. there is available/unassigned output port); see page. 8 , paragraph. 89-90).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-10, 16-23, and 34-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golla in view of Angle (U.S. 2003/0007498A1).

Regarding claim 1, 16 and 34, Golla discloses for use with a switch (see FIG. 1, network switch element 10) including a first number of output ports (see FIG. 1, Egress ports 15-1 to 15-N), a second number of input ports (see FIG. 1, ingress ports 18-1 to 18-N), and the first number of virtual output queues (see FIG. 1, VOQ-1 to VOQ-N) associated with each of the second number of input ports (see FIG. 1, each VOQ is coupled to each ingress port), a dispatch scheduler (see FIG. 1, a combined system of ingress server s 19-N, egress servers 14-N, scheduler arrangement 20 and matrix control 22 or see FIG. 7, a generalized scheduler 120) comprising:

a) a third number of subschedulers (see FIG. 1, a combined system of ingress servers/arbiters 19-1 to 19-H and egress servers/arbiters 14-1 to 14-H; see FIG. 5)

b) a first indicator (see FIG. 8, step 142, the request matrix R; see FIG. 12 B, request matrix), associated with each of the virtual output queues (see FIG. 12b, the request matrix contains/associates with each VOQ), for indicating whether the virtual output queue is storing a cell awaiting dispatch arbitration (see FIG. 12C, the requests in the request matrix

indicates the transmission units waiting to be served/granted by the server/scheduler, and each VOQ stores the transmission units; see page 6, paragraph 65-66; see page 7, paragraph 85-86; page 8, paragraph 87-89); and

c) a second indicator (see FIG. 12B, the a combined matrix of Grants Matrix and scheduling matrix, see FIG. 8, step 146), for each of the subschedulers (see FIG. 12B, the combined matrix contains/associates with each ingress/egress server), indicating whether the subscheduler is reserved or available (see FIG. 12C, the combined matrix is used at the server/arbiter to indicate/determine whether to accept/grant the request, and the request is used to determine whether there is match with predetermine/stored/reserved output port in the server or no match (i.e. there is available/unassigned output port); see page. 8 , paragraph. 89-90),

wherein each of the subschedulers is adapted to perform a matching operation (see FIG. 8, step 144 and 148, 150; each server performs matching process), if it has been reserved (see FIG. 146, step 146, note that matching process is performed based upon the predetermine/stored/reserved output port in the grant matrix), to match a cell buffered at a virtual output queue with its corresponding output port (see FIG. 8, step 146,150; note that the matching is performed between VOQ and the egress port; see page 6, paragraph 66-71; see page 7, paragraph 83-86; see page 8, paragraph 91-94),

wherein each of the subschedulers requires cell time slot to generate a match from its matching operation (see page 3, paragraph 44; note that time slot is utilized by the combined ingress/egress servers to perform matching process and to generate a grant to the request), and wherein the subschedulers can collectively generate a match result for each output port in

each cell time slot (see page 3, paragraph 44, see page 7, paragraph 79-80; note that each time slot is associated with a matrix cycle, and at each time slot, the combined system of scheduler performs a matching process and computes a matching result/product for each egress ports); and

fairness is maintained for best-effort traffic (see page 3, paragraph 44; see page 4, paragraph 52, see page 7, paragraph 85; page 14, paragraph 153,156; note that the scheduling algorithm utilizes the VOQs and servers in order to provide the fair scheduling. Moreover, the transmission units are best-effort traffic since it accepts the fair scheduling.)

Golla does not explicitly disclose wherein the subschedulers require more than one cell time slot to generate matching operation.

However, the above-mentioned claimed limitations are taught by Angle. In particular, Angle teaches a pipeline staging scheduling (see FIG. 11 A, pipeline scheduling process; see page 10, paragraph 112-113) and wherein each of the subschedulers (see FIG. 11A, multicast scheduling, unicast scheduling and combined scheduling) requires more than one cell time slot to generate a match from its matching/scheduling operation (see page 11, paragraph 115-116; by utilizing the pipeline scheduling process, the scheduler performs the scheduling operation in more than one time slot, to generate select/grant to the request.) and

In view of this, having the system of Golla and then given the teaching of Angle, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Golla, by providing the pipeline scheduler performing the scheduling process in more than one time slot, as taught by Angle. The motivation to combine is to obtain the advantages/benefits taught by Angle since Angle states at page 1,

paragraph 3-9 that such modification would provide efficient unicast and multicast scheduling and high throughput for traffic.

Regarding claims 2, 17 and 35, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Angle further teaches the third number of cell time slots to generate its matching/scheduling operation (see page 11, paragraph 116; note that the scheduling is performed more than one time slot in pipeline scheduling. Thus, it is clear that a number of time slots which are more than one time slots (i.e. two, three, and etc.) is utilized/required to perform scheduling/matching.)

In view of this, having the system of Golla and then given the teaching of Angle, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Golla, as taught by Angle, for the same motivation that stated above in Claims 1, 18 and 29.

Regarding claims 3, 18 and 36, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above.

Neither Golla nor Angle explicitly discloses no more than third number of cell time slots. Golla teaches the scheduling/mapping process is performed in one time slot. Angle teaches scheduling/mapping process is performed in more than one time slot in pipeline scheduling, wherein the number of time slots is more than one (i.e. two, three, etc.). Setting

the scheduling the time slot to a specific number of time slots does not define a patentable distinct invention over that in the combined system of Golla and Angle since both the invention as a whole and the combined system of Golla and Angle are directed to setting time slots to perform scheduling/mapping for sending the transmission units/packet in order to maintain the fairness. The degree in which setting the specific number of time slots presents no new or unexpected results, so long as the scheduling is processed within the specified time slots, the transmission units is processed in a successful way. If one has less number of server/scheduler/arbiter, it will require lesser number of time slots, and one has more number of server/scheduler/arbiter, it will require more number of time slots. The requirement is set according to the number schedulers/servers in pipeline scheduling system. Therefore, to have a specific number of time slots (i.e. no more than third number of slots) for pipeline scheduling process would have been routine experimentation and optimization in the absence of criticality.

Regarding claims 4 and 19, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Golla further discloses fairness is maintained for best-effort traffic (see page 3, paragraph 44; see page 4, paragraph 52, see page 7, paragraph 85; page 14, paragraph 153,156; note that the scheduling algorithm utilizes the VOQs and servers in order to provide the fair scheduling. Moreover, the transmission units are best-effort traffic since it accepts the fair scheduling.)

Regarding claims 5, 20 and 37, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Angle further discloses a matching operation selected from a group of matching operations consisting of (A) DRRM, and (B) iSLIP (see page 3, paragraph 43; note that a scheduler is implemented with iSLIP algorithm).

In view of this, having the system of Golla and then given the teaching of Angle, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Golla, by providing isLIP algorithm to the scheduler, as taught by Angle, for the same motivation that stated above in Claims 1,18 and 34.

Regarding claims 6 and 21, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Golla further discloses d) if a cell buffered at a virtual output queue has been successfully matched with its corresponding output port, informing the virtual output queue (see page 8, paragraph 90-91; see page 7, paragraph 76-78; note that upon detecting and matching a request in the grant matrix, the grant message is send to the requested VOQ of the ingress port.)

Regarding claims 7, 9, and 22, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Golla further discloses e) for each of the virtual output queues, if the virtual output queue has been informed that it has been successfully matched with its corresponding output

port (see page 8, paragraph 90-91; see page 7, paragraph 76-78; note that upon detecting and matching a request in the grant matrix, the grant message is send to the requested VOQ of the ingress port), then dispatching its head of line cell (see page 8, paragraph 91-93; see page 3, paragraph 41; see page 14, paragraph 158; not that the purpose of scheduling by utilizing VOQs is to avoid Head of the line blocking. Thus, it is clear the upon receiving the grant message, the transmission units/cell (see FIG. 12C, in port 0, q0) must be transmitted.)

Regarding claims 8, 10, and 23, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 1, 18, 34 as described above. Golla further discloses wherein the head of line cell is dispatched in a next cell time slot (see page 3, paragraph 44; see page 4, paragraph 52; see page 14, paragraph 155; note that the scheduling system process the transmission unit in each time slot. The time slots are counted in sequential order or close cycle. Thus, it is clear that once the grant message is received, the transmission unit or the cell at the head of the request VOQ must be transmitted in next time slot.)

7. Claims 11-12, 24-25 and 30-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golla and Angle, as applied to claims 1,16,29 above, and further in view of Rusu (U.S. 6,141,323).

Regarding claim 11, 24 and 30, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 11, 24 and 30 as described above, and Golla further teaches wherein the first indicator (see FIG. 1, Request matrix), for

each of the virtual output queues, for indicating whether the virtual output queue is storing a cell awaiting dispatch.

Neither Angle nor Angle discloses is a count (see FIG. 3, Diff. Measurement counter n 120), wherein the count is incremented upon learning that a new cell has arrived at the virtual output queue (see Rusu FIG. 3, Queue n 101; see col. 6, lines 33-62; note that the arrival of a cell to the queue causes the increments to the counter by one).

However, the above-mentioned claimed limitations are taught by Rusu. In view of this, having the combined system of Golla and Angle, then given the teaching of Rusu, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Golla and Angle, by providing a cell counter to measure the queue, as taught by Rusu. The motivation to combine is to obtain the advantages/benefits taught by C since Rusu states at col. 2, line 5-32 that such modification would to provide more complete and comprehensive information on the available storage capacity and rate of utilization of the queue on an ongoing basis.

Regarding claim 12, 25 and 31, the combined system of Golla and Angle discloses all aspects of the claimed invention set forth in the rejection of Claim 11, 24 and 30 as described above, and Golla further teaches an available subscheduler is reserved for considering a head of line cell at a corresponding virtual output queue (see page 8, paragraph 90-91; see page 7, paragraph 76-78; note that upon detecting and matching a request in the grant matrix, the grant message is send to the requested VOQ of the ingress port. Also, see page 8, paragraph 91-93; see page 3, paragraph 41; see page 14, paragraph 158; not that the purpose of

scheduling by utilizing VOQs is to avoid Head of the line blocking. Thus, it is clear that upon receiving the grant message, the transmission units/cell (see FIG. 12C, in port 0, q0) is accepted/reserved in order to transmit).

Neither Angle nor Angle discloses wherein the count is increment for considering a head of line cell at a queue (see Rusu FIG. 3, Queue n 101; see col. 6, lines 33-62; note that the departure of a cell to the queue causes the decrement to the counter by one).

However, the above-mentioned claimed limitations are taught by Rusu. In view of this, having the combined system of Golla and Angle, then given the teaching of Rusu, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Golla and Angle, by providing a cell counter to measure the queue, as taught by Rusu. The motivation to combine is to obtain the advantages/benefits taught by C since Rusu states at col. 2, line 5-32 that such modification would to provide more complete and comprehensive information on the available storage capacity and rate of utilization of the queue on an ongoing basis.

8. Claim 13-15, 26-28, 32 and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Golla and Angle as applied to claims 1, 16, and 29 above, and further in view of Chong (U.S. 6,657,959).

Regarding claims 13, 26 and 32, the combined system of Golla and Angle discloses wherein the second indicator, for each of the subschedulers, is set to indicate that the associated subscheduler is reserved and the first indicator indicates that a corresponding

virtual output queue is storing a cell awaiting dispatch arbitration set forth in the rejection of Claim 1, 16 and 29 as described above.

Neither Golla nor Angle discloses indicating the subscheduler is reserved if the corresponding output is waiting to dispatch a cell.

However, the above-mentioned claimed limitations are taught by Chong. In particular, Chong teaches wherein the second indicator, for the subscheduler (see FIG. 3A, entries in the ACR bitmap table), is set to indicate that the associated subscheduler is reserved (see FIG. 3A, occupied with VCw) if the first indicator (see FIG. 3A, entries in the Schedule Table 202) indicates that a corresponding output is storing a connection/cell awaiting to dispatch arbitration (see col. 5, lines 40-55; note that entries in the ACR bitmap table corresponds to entries in the schedule table. ACR bitmap is set to indicate that the a time slot in the scheduling table is occupied/reserved if the schedule table 202 indicates VCw in the schedule table for a transmission.)

In view of this, having the combined system of Golla and Angle, then given the teaching of Chong, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Golla and Angle, by providing a mechanism of indicating if there is the channel is occupied for transmission, as taught by Chong. The motivation to combine is to obtain the advantages/benefits taught by Chong since Chong states at col. 1, line 57-67 that such modification would provide enhanced scheduling capabilities and increased throughput.

Regarding claims 14, 27 and 33, the combined system of Golla and Angle discloses wherein the second indicator, for each of the subschedulers, is set to indicate that the associated subscheduler is available and the associated subscheduler matches a cell buffered at a virtual output queue with its corresponding output port (see FIG. 8, step 150, no more remaining requests; see page 6, paragraph 68; note that once the scheduler matches all requests and there are no remaining requests since all requests are buffered/queued and transmitted, then the scheduler must be available/free) set forth in the rejection of Claim 1, 16 and 29 as described above.

Neither Golla nor Angle discloses indicating the subscheduler is available if the corresponding output is buffered and dispatch a cell.

However, the above-mentioned claimed limitations are taught by Chong. In particular, Chong teaches wherein the second indicator, for the subscheduler (see FIG. 3A, entries in the ACR bitmap table), is set to indicate that the associated subscheduler is available (see FIG. 3A, set to 0 to indicate empty in the schedule table) if corresponding output is buffered and dispatch a connection/cell (see col. 5, lines 40-55; note that entries in the ACR bitmap table corresponds to entire in the schedule table. ACR bitmap is set to indicate that a time slot in the scheduling table is empty if the schedule table 202 is available. There are no entries to be serviced).

In view of this, having the combined system of Golla and Angle, then given the teaching of Chong, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Golla and Angle, by providing a mechanism of indicating if there is the channel is occupied for transmission, as

taught by Chong for the same purpose and modification as described above in claims 13,26, and 32.

Regarding claims 15 and 28, the combined system of Golla and Angle discloses wherein the second indicator, for each of the subschedulers, is set to indicate that the associated subscheduler is reserved and the first indicator indicates that a corresponding virtual output queue is storing a cell awaiting dispatch arbitration and subscheduler generates a match result in each time slot set forth in the rejection of Claim 1, 16 and 29 as described above. Golla discloses a kth subscheduler and kth is set to third number (see FIG. 1, a combined system of ingress servers/arbiters 19-1 to 19-H and egress servers/arbiters 14-1 to 14-H; see FIG. 5, thus the number of combined servers H=k). Angle further teaches utilizing the plurality of cell time slots to generate its matching/scheduling operation (see page 11, paragraph 116; note that the scheduling is performed more than one time slot in pipeline scheduling. Thus, it is clear that a number of time slots which are more than one time slots (i.e. two, three, and etc.) is utilized/required to perform scheduling/matching.)

Neither Golla nor Angle discloses indicating the subscheduler is reserved if the corresponding output is waiting to dispatch a cell.

However, the above-mentioned claimed limitations are taught by Chong. In particular, Chong teaches wherein the second indicator, for the subscheduler (see FIG. 3A, entries in the ACR bitmap table), is set to indicate that the associated subscheduler is reserved (see FIG. 3A, occupied with VCw) if the first indicator (see FIG. 3A, entries in the Schedule Table 202) indicates that a corresponding output is storing a connection/cell

awaiting to dispatch arbitration (see col. 5, lines 40-55; note that entries in the ACR bitmap table corresponds to entries in the schedule table. ACR bitmap is set to indicate that the a time slot in the scheduling table is occupied/reserved if the schedule table 202 indicates VCw in the schedule table for a transmission.)

In view of this, having the combined system of Golla and Angle, then given the teaching of Chong, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the combined system of Golla and Angle, by providing a mechanism of indicating if there is the channel is occupied for transmission, as taught by Chong. The motivation to combine is to obtain the advantages/benefits taught by Chong since Chong states at col. 1, line 57-67 that such modification would provide enhanced scheduling capabilities and increased throughput.

Neither Golla nor Angle explicitly discloses k is set the current time slot modulo the third number. Golla teaches the scheduling/mapping process is performed in one time slot and a kth subscheduler, thus kth scheduler must be performed in current time slot. Angle teaches scheduling/mapping process is performed in more than one time slot in pipeline scheduling, wherein the number of time slots is more than one (i.e. two, three, etc.), for plurality of schedulers. Setting the scheduling the time slot to a specific number of time slots in accordance with the number of servers/schedulers does not define a patentable distinct invention over that in the combined system of Golla, Angle and Chong since both the invention as a whole and the combined system of Golla, Angle and Chong are directed to setting the number time slots (i.e. current time slot modulo the third number) in accordance to the numbers servers (i.e. k; in particular, k= current time slot modulo third number) to

perform scheduling/mapping for sending the transmission units/packet in order to maintain the fairness. The degree in which setting the specific number of time slots in accordance to a number of servers the presents no new or unexpected results, so long as the scheduling is processed within the specified time slots by the specified number of servers, the transmission units is processed in a successful way. Since the number of servers reflects the number of time slots, if one has less number of server/scheduler/arbiter, it will require lesser number of time slots, and one has more number of server/scheduler/arbiter, it will require more number of time slots. A specific time slot requirement is set according to the number schedulers/servers in pipeline scheduling system. Therefore, to have a specific number of servers (i.e. k) set to a specific number of time slots (i.e. current time slot modulo the third number) for pipeline scheduling process would have been routine experimentation and optimization in the absence of criticality.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ian N Moore whose telephone number is 571-272-3085. The examiner can normally be reached on M-F: 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Vanderpuye can be reached on 571-272-3078. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

INM
10/22/04

BRIAN NGUYEN
PRIMARY EXAMINER